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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/746,068	12/26/2000	Hisashige Ando	1614.1107	1994

21171 7590 05/26/2005

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/746,068	ANDO, HISASHIGE	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-19* is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *11 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-16 remain for examination. Claims 17-19 are newly added.

2. Claims 17-19 are newly combined features of previously objected claims , and are therefore, allowable over the art of record for the reason set forth in paragraphs 23-25 in the previous action on 06/03/04.

3. This action also included a new ground of rejections based on newly amended claims 1,9.

4. Applicant's arguments with respect to claims 1-16, particularly regarding the issue of separate and independent processes, have been considered but are moot in view of the new ground(s) of rejection. The reasons are given below :

5. Helenius (4,395,758) and Hennessy were already cited to applicant in a previous action, therefore, copies are not provided herein.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1,2,6 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Helenius (4,395,758) in view of George Hoff (3,631,405) .

7. Helenius taught system that executes a specific process more frequently than other processes among a variety of processes said information-processing device comprising:

a) corresponding to the variety of processes', Column 2, lines 30-45 show a central

a first processor configured to execute an entire instruction set processor or first processor for processing a number of instructions (an entire instruction set).

b) a second processor configured to execute a portion or entirety of the same instruction set that the first processor executes, said second processor being capable of executing a part of said instruction set corresponding to the specific process more efficiently than said first processor', This section also shows that a special processor processes certain of those instructions (a portion of the same instruction set). This processor is the floating point accelerator mentioned in column 12, lines 19-23 and column 13, lines 17-19 that processes these special instructions (floating point instructions) more efficiently, especially when extensive floating point instructions are used (the more frequently executed specific process as opposed to the other instructions).

c) wherein said second processor executes the specific process whereas said first processor executes the other processes, as shown above.

8. Helenius did not specifically show the execution of independent and separate processes by first and second processors as claimed. However, Hoff disclosed separate and independent processes executed by a first processor and sound processor (see program processed by p1 and program processed by p2 in fig.1) . It would have been obvious to one of ordinary skill in the art to use Hoff in Helenius for including the separate and independent processing as claimed because the use of Hoff could provide Helenius the ability to execute instructions by multiple processors at a

given cycle, and thereby increasing the bandwidth of the processing level, and because Helenius taught also the execution of repeated instructions which required significant periods of time (col.2, lines 24-30), which was an indication of the need of providing multiple processors to process instructions independently in order to reduce the extra cycle caused by the repeated instructions, and therefore, in doing so, provided a motivation.

9. As to claim 2, Helenius disclosed all the processes are allocated to said second processor initially, wherein said second processor passes a given process to said first processor by interrupting said first processor in a case in which an instruction other than the part of the instruction set corresponding to the specific process must be executed. Column 2, lines 37-43 show that all operands (and thus the processes) are allocated to the special processor. If the special processor determines that the instructions are special instructions (floating point) that it should execute, it inhibits or interrupts the first processor from processing the operation.

10. As to claim 6, Helenius discloses the information-processing device as claimed in claim 1, as described above, wherein said first processor is a general-purpose processor, wherein said second processor is a transaction processor designed to efficiently execute a transaction process as the specific process. The abstract shows that the central processor has general purpose registers and is thus a general purpose processor. Figure 9 shows that the special processor (100) performs transactions with

the central processor and thus is a transaction processor.

11. As to claim 7, Helenius discloses the information-processing device as claimed in claim 1 , as described above, wherein said first processor and said second Processor Share a memory Space. As shown in the section cited above, the processor and special processor receive instruction information of the same instruction at the same time and thus are accessing the same memory.

Claim Rejections - 35 USC f 103

12. Claims 5, 8-1 1, and 13-16 are rejected under 35 U.S.C. 1O3(a) as being

13. unpatentable over Helenius in view George Hoff (3,631,405) . as applied to claims 1,3,6,7, and further in view of in view of Hennessy.

14. As to claim 5, as described above, wherein said second processor is capable of executing the part of said instruction set corresponding to the specific process more Helenius discloses the information-processing device as claimed in claim efficiently than said first processor (as described above), specific process more efficiently by executing said specific process in parallel by Helenius does not disclose that the second processor executes the use of at least one of a multi-threading method and a multi-processing method.

15. Hennessy has disclosed on page 718 in figure 9.2 a multiprocessor for increasing efficiency by parallel processing. It is defined page 712, last

paragraph that a parallel processing program is a program that runs on multiple processors, thus the processors run in parallel. Hennessy has taught on page 712 that computers are made more powerful by connecting many small ones or by multiprocessing. It also says that multiprocessors may be faster than the fastest uniprocessor. This notable processing speed increase would have motivated one of ordinary skill in the art to modify the design of Helenius to make the second processor a multiprocessor as taught by Hennessy. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Helenius to make the second processor execute in parallel by making it a multiprocessor as taught by Hennessy so that execution is faster and more efficient.

16. As to claim 8, Helenius does not disclose wherein said information-processing device increasing efficiency by parallel processing. Hennessy has taught on page 712 that computers are made more powerful by connecting many small ones or by multiprocessing. It also says that multiprocessors may be faster than the fastest uniprocessor. This notable processing speed increase would have motivated one of ordinary skill in the art to modify the design of Helenius to make the first and second processors multiprocessors as taught by Hennessy. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Helenius to make the first and second processors multiprocessors as taught by Hennessy so that execution is faster and more powerful.

17. As to claim 9, Helenius discloses an information-processing device (figure 2) that corresponding to the variety of processes', Column 2, lines 30-45 show a central processor or first processor for processing a number of instructions (an entire instruction set). a second processor configured to execute a potion or entirety of the same instruction set that the first processor executes, said second processor being capable of executing a pad of said instruction set corresponding to the specific process more efficiently than said first processor', This section also shows that a special processor processes certain of those instructions (a portion of the same instruction set). This processor is the floating point accelerator mentioned in column 12, lines 19-23 and column 13, lines 17-19 that processes these special instructions (floating point instructions) more efficiently, especially when extensive floating point instructions are used (the more frequently executed specific process as opposed to the other instructions). wherein said second processor executes the specific process whereas said first processor executes the other processes as shown above. Helenius does not disclose that the second processor is capable of executing multiples of a specific process concurrently. Hennessy has disclosed on page 718 in figure 9.2 a multiprocessor for increasing efficiency by parallel processing. It is defined page 712, last paragraph that a parallel processing program is a program that runs on multiple processors, thus the processors run in parallel. This means that if applied to the system of Helenius, the process that the second processor executes would be run on multiple processors, or multiples of the process would be executed. Hennessy has taught on page 712 that computers are made more powerful by connecting many small ones or by

multiprocessing. It also says that multiprocessors may be faster than the fastest uniprocessor. This notable processing speed increase would have motivated one of ordinary skill in the art to modify the design of Helenius to make the first and second processors multiprocessors as taught by Hennessy. It would have been obvious to one of ordinary skill in the ad at the time of invention to modify the design of Helenius to make the first and second processors multiprocessors as taught by Hennessy so that execution is faster and more powerful.

18. As to claim 10, Helenius in view of Hennessy discloses the information-processing device as claimed in claim 9, as shown above, wherein all the processes are allocated to said second processor initially, wherein said second processor passes a given process to said first processor in a case in which an instruction other than the pad of the instruction set corresponding to the specific process must be executed. Column 2, lines 37-43 show that all operands (and thus the processes) are allocated to the special processor. If the special processor determines that the instructions are special instructions (floating point) that it should execute, it inhibits or interrupts the first processor from processing the operation.

19. As to claim 11, Helenius in view of Hennessy discloses the information-processing device as claimed in claim 9, as described above, wherein all the processes are allocated to said second processor initially, wherein said second processor passes a given process to said first processor when an instruction that cannot be executed appears or the execution of the process is judged not efficient by said second processor in said given process. Since the second processor would have decided to execute the

instruction and inhibit the first processor and because the architecture of the patent is designed for the second processor to more efficiently process the special instructions than the first processor, when the second processor does not inhibit the first processor and sends the operands to the first processor, the second processor inherently judges the process not efficient.

20. As to claim 13, Helenius in view of Hennessy discloses the information-processing device as claimed in claim 9, as described above, wherein said second processor is capable of executing all or part of said instruction set corresponding to the specific process more efficiently than said first processor (as described above)

21. Helenius in view of Hennessy does not disclose that the second processor executes the specific process more efficiently by executing said specific process in parallel by use of at least one of a multi-threading method and a multi-processing method.

22. Hennessy has disclosed on page 718 in figure 9.2 a multiprocessor for increasing efficiency by parallel processing. It is defined page 712, last paragraph that a parallel processing program is a program that runs on multiple processors, thus the processors run in parallel., and more powerful by connecting many small ones or by multiprocessing. It also says that multiprocessors may be faster than the fastest uniprocessor. This notable Hennessy has taught on page 712 that computers are made more processing speed increase would have motivated one of ordinary skill in the art to modify the design of Helenius in view of Hennessy to make the second processor a multiprocessor as taught by Hennessy.

23. It would have been obvious to one of ordinary skill in the ad at the time of invention to modify the design of Helenius in view of Hennessy to make the second processor execute in parallel by making it a multiprocessor as taught by Hennessy so that execution is faster and more efficient.

24. As to claim 14, Helenius in view of Hennessy discloses the information-processing device as claimed in claim 9, as described above, wherein said first processor is a general-purpose processor, wherein said second processor is a transaction processor designed to efficiently execute a transaction process as the specific process. The abstract shows that the central processor has general purpose registers and is thus a general purpose processor. Figure 9 shows that the special processor (100) performs transactions with the central processor and thus is a transaction processor.

25. As to claim 15, Helenius in view of Hennessy discloses the information-processing device as claimed in claim 9, as described above, wherein said first processor and said second processor share common memory address space. As shown in the section cited above, the processor and special processor receive

26. AS to claim 16, Helenius does not disclose wherein said information-processing device includes a plurality of first processors and second processors, increasing efficiency by parallel processing. Hennessy has taught on page 712 that computers are made more Helenius discloses the information-processing device as claimed in claim

Hennessy has disclosed on page 718 in figure 9.2 a multiprocessor for powerful by connecting many small ones or by multiprocessing. It also says that multiprocessors may be faster than the fastest uniprocessor. This notable processing speed increase would have motivated one of ordinary skill in the art to modify the design of Helenius to make the first and second processors multiprocessors as taught by Hennessy. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Helenius to make the first and second processors multiprocessors as taught by Hennessy so that execution is faster and more powerful.

27. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior ad of record does not specifically teach the second processor interrupting the first processor to execute a process when the second processor cannot execute or efficiently execute the process. Instead, the first processor is simply not inhibited in doing so. In addition, no prior art of record suggests that it would have been obvious to one of ordinary skill in the art at the time of invention to modify the prior art of record so the second processor interrupts the first processor to execute a process when the second processor cannot execute or efficiently execute the process.

28. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base

claim and any intervening claims. The prior art of record does not specifically teach that the process the second instruction cannot execute efficiently is a floating point pr process. Instead, the second processor does efficiently execute these processes. In addition, no prior art of record suggests that it would have been obvious to one of ordinary skill in the art at the time of invention to modify the prior art of record so the process the second instruction cannot execute efficiently is a floating point process.

29. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant's amendment (to claims 1,9) necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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